

What is claimed is:

1. An apparatus for current balance in a multi-phase
DC-to-DC converter having a converter output for providing an
output voltage and a plurality of channels each configured for
generating a channel current, said apparatus comprising:

a voltage sense circuit for sensing said output voltage and
generating a voltage sense signal;

a plurality of current sense circuits each corresponding to one
of said plurality of channels for sensing said channel
current and generating a current sense signal for said
corresponding channel;

a comparator for receiving said voltage sense signal and a
reference signal and generating an error signal; and

a plurality of multi-input pulse width modulators each for
generating a PWM signal for regulating said channel
current of said corresponding channel by a first input
pair comparing said error signal with a ramp signal and
one or more second input pair each comparing said
current sense signal of said corresponding channel with
each other of said plurality of current sense signals.

2. An apparatus according to claim 1 wherein each of said
plurality of multi-input pulse width modulators comprises:

a current mirror including a reference branch and a mirror

branch for generating a differential signal from said mirror branch;

a first input stage including a positive input for receiving said error signal and a negative input for receiving said ramp signal, said positive and negative input corresponding to said reference branch and mirror branch respectively;

one or more second input stage each including a positive input and a negative input corresponding to said reference branch and mirror branch respectively, each of said negative inputs receiving said current sense signal of said corresponding channel, each of said positive inputs receiving one of said plurality of current sense signals other than said current sense signal of said corresponding channel;

a plurality of current sources each providing a bias current for one of said first and second input stages; and
a gain stage for amplifying said differential signal.

3. An apparatus according to claim 1 wherein each of said plurality of multi-input pulse width modulators comprises:

a first and second load device connecting to a power supply for providing a positive and negative branch and generating a positive and negative branch signal respectively;

a first input stage including a positive input for receiving said

error signal and a negative input for receiving said ramp
signal, said positive and negative input corresponding
to said positive and negative branch respectively;
one or more second input stage each including a positive
input and a negative input corresponding to said
positive and negative branch respectively, each of said
negative inputs receiving said current sense signal of
said corresponding channel, each of said positive inputs
receiving one of said plurality of current sense signals
other than said current sense signal of said
corresponding channel;
a plurality of current sources each providing a bias current for
one of said first and second input stages; and
a gain stage for amplifying a difference between said positive
and negative branch signal.

4. An apparatus according to claim 1 wherein each of said
plurality of current sense signals is a voltage type signal.

5. An apparatus according to claim 1 wherein each of said
plurality of current sense signals is a current type signal.

6. An apparatus according to claim 1 wherein each of said
plurality of current sense circuits includes a high-side and low-side
transistor connected in series between a high-side and low-side

voltage for generating said current sense signal derived from an interconnection between said high-side and low-side transistor.

7. An apparatus for current balance in an N-phase DC-to-DC
5 converter having a converter output for providing an output voltage and N channels each configured for generating a channel current, said apparatus comprising:

a voltage sense circuit for sensing said output voltage and
generating a voltage sense signal;

10 N current sense circuits each corresponding to one of said N channels for sensing said channel current and generating a current sense signal for said corresponding channel;

15 a first comparator for receiving said voltage sense signal and a reference signal and generating an error signal;

N second comparators each for generating a combined signal by a negative input receiving N-1 times of said current sense signal of said corresponding channel and N positive inputs receiving said error signal and said N current sense signals other than said current sense signal of said corresponding channel; and

20 N pulse width modulators each for generating a PWM signal for regulating said channel current of said corresponding channel by receiving said combined signal and a ramp signal.

25

8. An apparatus according to claim 7 wherein each of said pulse width modulators comprises:

a current mirror including a reference branch and a mirror branch for generating a differential signal from said mirror branch;

an input stage including a positive input for receiving said combined signal corresponding to said reference branch and a negative input for receiving said ramp signal corresponding to said mirror branch;

a current source for providing a bias current for said input stage; and

a gain stage for amplifying said differential signal.

9. An apparatus according to claim 7 wherein each of said pulse width modulators comprises:

a first and second load device connecting to a power supply for providing a positive and negative branch and generating a positive and negative branch signal respectively;

an input stage including a positive input for receiving said combined signal corresponding to said positive branch and a negative input for receiving said ramp signal corresponding to said negative branch ;

a current source for providing a bias current for said input stage; and

a gain stage for amplifying a difference between said positive and negative branch signal.

10. An apparatus according to claim 7 wherein each of said
5 second comparators comprises:

a first transistor for receiving said current sense signal of said
corresponding channel;

N-1 second transistor for receiving said current sense signals
other than said current sense signal of said
10 corresponding channel respectively; and

a common bias for said first and second transistors;
wherein said first transistor is N-1 times of said second
transistor in size.

11. An apparatus according to claim 7 wherein each of said
15 current sense signals is a voltage type signal.

12. An apparatus according to claim 7 wherein each of said
current sense signals is a current type signal.

20 13. An apparatus according to claim 7 wherein each of said
current sense circuits includes a high-side and low-side transistor
connected in series between a high-side and low-side voltage for
generating said current sense signal derived from an
25 interconnection between said high-side and low-side transistor.

14. An apparatus for current balance in an N-phase DC-to-DC converter having a converter output for providing an output voltage and N channels each configured for generating a channel current,
5 said apparatus comprising:

a voltage sense circuit for sensing said output voltage and
generating a voltage sense signal;

N current sense circuits each corresponding to one of said N
channels for sensing said channel current and
generating a current sense signal for said
10 corresponding channel;

a first comparator for receiving said voltage sense signal and a
reference signal and generating an error signal;

N second comparators each for generating a combined signal
by a negative input receiving N times of said current
sense signal of said corresponding channel and N+1
positive inputs receiving said error signal and said N
15 current sense signals; and

N pulse width modulators each for generating a PWM signal
for regulating said channel current of said
20 corresponding channel by receiving said combined
signal and a ramp signal.

15. An apparatus according to claim 14 wherein each of said
25 pulse width modulators comprises:

a current mirror including a reference branch and a mirror branch for generating a differential signal from said mirror branch;

an input stage including a positive input for receiving said combined signal corresponding to said reference branch and a negative input for receiving said ramp signal corresponding to said mirror branch;

a current source for providing a bias current for said input stage; and

a gain stage for amplifying said differential signal.

16. An apparatus according to claim 14 wherein each of said pulse width modulators comprises:

a first and second load device connecting to a power supply for providing a positive and negative branch and generating a positive and negative branch signal respectively;

an input stage including a positive input for receiving said combined signal corresponding to said positive branch and a negative input for receiving said ramp signal corresponding to said negative branch ;

a current source for providing a bias current for said input stage; and

a gain stage for amplifying a difference between said positive and negative branch signal.

17. An apparatus according to claim 14 wherein each of said second comparators comprises:

a first transistor for receiving said current sense signal of said corresponding channel;

5 N second transistor for receiving said current sense signals respectively; and

a common bias for said first and second transistors;

wherein said first transistor is N times of said second transistor in size.

10 18. An apparatus according to claim 14 wherein each of said current sense signals is a voltage type signal.

15 19. An apparatus according to claim 14 wherein each of said current sense signals is a current type signal.

20 20. An apparatus according to claim 14 wherein each of said current sense circuits includes a high-side and low-side transistor connected in series between a high-side and low-side voltage for generating said current sense signal derived from an interconnection between said high-side and low-side transistor.

25 21. An apparatus for current balance in an N-phase DC-to-DC converter having a converter output for providing an output voltage and N channels each configured for generating a channel current,

said apparatus comprising:

a voltage sense circuit for sensing said output voltage and generating a voltage sense signal;

5 N current sense circuits each corresponding to one of said channels for sensing said channel current and generating a current sense signal for said corresponding channel;

a first comparator for receiving said voltage sense signal and a reference signal and generating an error signal;

10 N second comparators each for generating a combined signal by subtracting N-1 times of said current sense signal of said corresponding channel from said error signal and current sense signals other than said current sense signal of said corresponding channel; and

15 N pulse width modulators each for generating a PWM signal for regulating said channel current of said corresponding channel by receiving said combined signal and a ramp signal.

20 22. An apparatus according to claim 21 wherein each of said pulse width modulators comprises:

a current mirror including a reference branch and a mirror branch for generating a differential signal from said mirror branch;

25 an input stage including a positive input for receiving said

combined signal corresponding to said reference branch
and a negative input for receiving said ramp signal
corresponding to said mirror branch;
a current source for providing a bias current for said input
stage; and
a gain stage for amplifying said differential signal.

23. An apparatus according to claim 21 wherein each of said
pulse width modulators comprises:
a first and second load device connecting to a power supply for
providing a positive and negative branch and generating
a positive and negative branch signal respectively;
an input stage including a positive input for receiving said
combined signal corresponding to said positive branch
and a negative input for receiving said ramp signal
corresponding to said negative branch ;
a current source for providing a bias current for said input
stage; and
a gain stage for amplifying a difference between said positive
and negative branch signal.

24. An apparatus according to claim 21 wherein each of said
second comparators comprises:
a first transistor for receiving said current sense signal of said
corresponding channel;

N-1 second transistor for receiving said current sense signals
other than said current sense signal of said
corresponding channel respectively; and
a common bias for said first and second transistors;
5 wherein said first transistor is N-1 times of said second
transistor in size.

25. An apparatus according to claim 21 wherein each of said
second comparators comprises:

a first transistor for receiving said current sense signal of said
corresponding channel;

N second transistor for receiving said current sense signals
respectively; and

a common bias for said first and second transistors;

10 wherein said first transistor is N times of said second
transistor in size.

26. An apparatus according to claim 21 wherein each of said
current sense signals is a voltage type signal.

20 27. An apparatus according to claim 21 wherein each of said
current sense signals is a current type signal.

28. An apparatus according to claim 21 wherein each of said
25 current sense circuits includes a high-side and low-side transistor

connected in series between a high-side and low-side voltage for generating said current sense signal derived from an interconnection between said high-side and low-side transistor.

5 29. A method for current balance in a multi-phase DC-to-DC converter having a converter output for providing an output voltage and a plurality of channels each configured for generating a channel current, said method comprising the steps of:

sensing said output voltage to thereby determine a voltage sense signal;

sensing each of said plurality of channel currents to thereby determine a plurality of current sense signals;

comparing said voltage sense signal with a reference signal to thereby determine an error signal;

15 generating a plurality of PWM signals by a plurality of multi-input pulse width modulators each comparing said error signal with a ramp signal and one of said plurality of current sense signals with each other of said plurality of current sense signals; and
20 regulating said channel currents with said plurality of PWM signals.

30 30. A method according to claim 29 further comprising the steps of :

25 connecting a high-side and low-side transistor in series

between a high-side and low-side voltage; and
deriving from an interconnection between said high-side and
low-side transistor to thereby determine said current
sense signal.

5

31. A method for current balance in a multi-phase DC-to-DC
converter having a converter output for providing an output voltage
and a plurality of channels each configured for generating a channel
current, said method comprising the steps of:

sensing said output voltage to thereby determine a voltage
sense signal;

sensing each of said plurality of channel currents to thereby
determine a plurality of current sense signals;

comparing said voltage sense signal with a reference signal to
thereby determine an error signal;

further comparing said error signal with a ramp signal to
thereby determine a first differential signal;

generating a plurality of second differential signals each by
comparing a respective one of said plurality of current
sense signals with each other of said plurality of current
sense signals;

summing said first and second differential signals to thereby
determine a respective combined differential signal;

generating a plurality of PWM signals each responsive to said
respective combined differential signal; and

25

regulating said channel currents with said plurality of PWM signals.

32. A method according to claim 31 further comprising the
5 steps of:

connecting a high-side and low-side transistor in series
between a high-side and low-side voltage; and
deriving from an interconnection between said high-side and
low-side transistor to thereby determine said current
sense signal.

33. A method according to claim 31 further comprising the
steps of amplifying said respective combined differential signal.

34. A method for current balance in an N-phase DC-to-DC
converter having a converter output for providing an output voltage
and N channels each configured for generating a channel current,
said method comprising the steps of:

sensing said output voltage to thereby determine a voltage
sense signal;

sensing each of said channel currents to thereby determine N
current sense signals;

comparing said voltage sense signal with a reference signal to
thereby determine an error signal;

generating N PWM signals each derived from a respective

differential signal produced by subtracting a ramp
signal and N-1 times of a respective one of said current
sense signals from a summation of said error signal and
each other of said plurality of current sense signals; and
5 regulating said channel currents with said N PWM signals.

35. A method according to claim 34 further comprising the
steps of :

connecting a high-side and low-side transistor in series
between a high-side and low-side voltage; and
10 deriving from an interconnection between said high-side and
low-side transistor to thereby determine said current
sense signal.

36. A method according to claim 34 further comprising the
steps of amplifying said respective differential signal.

37. A method for current balance in an N-phase DC-to-DC
converter having a converter output for providing an output voltage
and N channels each configured for generating a channel current,
20 said method comprising the steps of:

sensing said output voltage to thereby determine a voltage
sense signal;

sensing each of said channel currents to thereby determine N
25 current sense signals;

comparing said voltage sense signal with a reference signal to
thereby determine an error signal;
subtracting N-1 times of a respective one of said current sense
signals from a summation of said error signal and each
other of said plurality of current sense signals to
thereby determine a respective combined signal;
generating N PWM signals each derived from a respective
differential signal produced by comparing said
respective combined signal with a ramp signal; and
regulating said channel currents with said PWM signals.

38. A method according to claim 37 further comprising the
steps of :

connecting a high-side and low-side transistor in series
between a high-side and low-side voltage; and
deriving from an interconnection between said high-side and
low-side transistor to thereby determine said current
sense signal.

39. A method according to claim 37 further comprising the
steps of amplifying said respective differential signal.